
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: MOSTAFAZADEH

Attorney Docket No.:
NSC1P194D1/P04836D1

Application No.: NEW

Examiner: UNASSIGNED

Filed: HEREWTHH

Group: UNASSIGNED

Title: CHIP SCALE PIN ARRAY

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR §§1.56 AND 1.97(c)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The references listed in the attached PTO Form 1449 may be material to examination of the above-identified patent application. Applicants submit the list of these references in compliance with their duty of disclosure pursuant to 37 CFR §§1.56 and 1.97. The Examiner is requested to make these references of official record in this application. The above-identified application is a Divisional of prior application U.S. Patent Application No. 09/698,736. This prior application is being relied upon for an earlier filing date under 35 U.S.C. § 120. Because the listed references were either cited by the PTO, or submitted to the PTO in the prior application, under 37 CFR § 1.98(d) Applicants submit that copies need not be provided.

This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that these references indeed constitute prior art.

This Information Disclosure Statement is believed to be filed before the mailing date of a first Office Action on the merits. Accordingly, it is believed that no fees are due in connection with the filing of this Information Disclosure Statement. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 50-0388 (Order No. NSC1P194D1).

Respectfully submitted,
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Form 1449 (Modified) Information Disclosure Statement By Applicant (Use Several Sheets if Necessary)	Atty Docket No.	Application No.:
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	Applicant:	
	MOSTAFAZADEH	
Filing Date	Group	
HEREWITH	UNASSIGNED	

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	1	6,261,864	7/17/01	Jung et al.			
	2	6,451,627	7/17/02	Coffman			
	3	6,306,685	10/23/01	Liu et al.			
	4	6,333,252	12/25/01	Jung et al.			
	5	5,656,550	8/12/97	Tsuji et al.			
	6	5,759,874	6/2/98	Okawa			
	7	5,585,195	12/17/96	Shmiada			
	8	6,034,422	3/7/00	Horita et al.			
	9	6,342,730	1/29/02	Jung et al.			
	10	6,238,952	5/29/01	Lin			
	11	5,895,234	04/99	Taniguchi et al.			
	12	6,100,594	08/00	Fukui et al.			
	13	6,355,507	03/02	Fanworth, Warren M.			
	14	6,177,288	01/01	Takiar, Hem P.			
	15	6,255,740	07/01	Tsuji et al.			
	16	5,866,948	02.02.99	Murakami et al.			
	17	6,258,626	07-2001	Wang et al.			
	18	6,157,080	12-2000	Tamaki et al.			
	19	6,247,229 B1	06/19/01	Glenn			
	20	6,358,778 B1	03/19/02	Shinohara			
	21	5,830,800	11/03/98	Lin			
	22	5,847,458	12/08/98	Nakamura et al.			
	23	5,923,080	07/13/99	Chun			
	24	5,998,875	12/07/99	Bodö			
	25	6,306,684 B1	10/23/01	Richardson et al.			
	26	6,307,755 B1	10/23/01	Williams et al.			
	27	6,316,837 B1	11/13/01	Song			
	28	6,130,473	10/10/00	Mostafazadeh et al.			

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No

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Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	29	U.S. Patent Application No. 09/528,540, entitled "Leadless Packaging Process Using a Conductive Substrate", filed March 20, 2000, inventor(s): Bayan et al.
	30	U.S. Patent Application No. 09/698,784, entitled "Flip Chip Scale Package", filed October 26, 2000, inventor(s): Shahram Mostafazadeh
	31	U.S. Patent Application No. 09/698,736, entitled "Chip Scale Pin Array", filed October 26, 2000, inventor(s): Shahram Mostafazadeh
Examiner		Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.